REMARKS

The Examiner rejected claim 9 under 35 USC §102(a) as being anticipated by applicant's admitted prior art, referring to the specification page 1, lines 12-16. The background section of the present application explains various processes by which silicon dioxide films can be pretreated to attempt to provide a smooth morphology. The process discussed in the specification at page 1, lines 12-16, involves the pretreatment of silicon dioxide films with hydrogen ions by using a Kaufman ion source. The Examiner asserts that the limitation of the hydrogen ions deposited by the plasma source ion implantation process is a product-by-process limitation and that the process for depositing the hydrogen ion is not structurally limiting.

An embodiment of the invention describes a semiconductor device precursor wherein hydrogen ions are deposited on the layer of silicon dioxide and the layer of polycrystalline silicon has a smooth morphology. The silicon dioxide layer of the present invention is free of metal contaminants. See amended claim 9 and the specification at page 2, lines 22-25, page 6, lines 21-25, and page 10, lines 6-14. Prior art was brought to the attention of the Examiner in order to point out a deficiency in the prior art process and product. As explained in the specification on page 1, lines 16-22, the surface morphology produced by the prior art process is contaminated with pieces of metal that become implanted in the target object. Amended claim 9 recites that the layer of silicon dioxide is free from metal contaminants. The prior art product is not. Amended claim 9 is patentable thereover.

The Examiner also rejected claims 10-12 under 35 USC §103(a) as being unpatentable over Burns et al. in view of applicant's admitted prior art. Burns et al. teaches a field effect transistor having a substrate with a layer of silicon dioxide over the substrate. In the rejection of claim 10, the Examiner asserts that the layer of silicon dioxide is covered by a layer of polycrystalline silicon and points to page 177 of Burns et al. However, Burns et al. teaches a thin layer of aluminum that is deposited on top of the silicon dioxide layer. See page 177. The Examiner also admits that Burns et al. does not teach implanting hydrogen ions into the silicon dioxide.

As explained above, the prior art teaches a silicon dioxide film that is pretreated with hydrogen ions, then covers with a layer of polycrystalline silicon to provide a thinner and smoother polycrystalline silicon film. The silicon dioxide is pretreated by ion beam bombardment by a Kaufman ion source which causes metal contamination.

Claim 10, as amended, recites a field effect transistor that includes "a layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of metal contamination in the layer." Burns et al. does not teach or suggest to implant the silicon dioxide film with hydrogen ions or a polycrystalline silicon layer. There is no teaching or suggestion in the admitted prior art to create a field effect transistor using the pretreated silicon dioxide layer. Furthermore, neither reference teaches or suggests a silicon dioxide layer which is free of metal contamination. Thus, amended claim 10 would not have been obvious.

The Examiner next rejected claim 11 pointing to pages 380-381 of Burns et al. in combination with applicant's admitted prior art in the specification on page 1, lines 12-15. Burns et al. teaches a read-only memory array wherein the field effect transistor is used. In the positions where a field effect transistor is desired, a thin oxide layer is formed and polysilicon rows act as an effective gate over the region the used for the field effect transistor. The admitted prior art is explained above.

Claim 11 recites a memory array which includes "a layer of silicon dioxide that having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free from metal contamination." Burns et al. does not teach or suggest using a layer of silicon dioxide that has been implanted with hydrogen ions or the need for a smooth morphology in the polycrystalline silicon layer. The admitted prior art does not even mention a memory array. Neither reference teaches or suggests a silicon dioxide layer which is free from metal contamination. Thus, claim 11, as amended, is nonobvious over Burns et al. in view of the admitted prior art.

The Examiner next rejects claim 12 asserting that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a

semiconductor wafer including a plurality of die. Claim 12 of the present invention describes a semiconductor wafer that includes a semiconductor substrate with a layer of silicon dioxide is formed on the semiconductor substrate. The layer of silicon dioxide has been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein the layer of silicon dioxide is free from metal contamination. The Examiner asserts that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. The Examiner further states that it is well known in semiconductor processing because multiple devices are formed on a single wafer and then split into individual die to allow for processing of a great number of die at one time to save costs.

As stated above, one of ordinary skill in the art would not know to form the transistor of amended claim 10 or the memory array of amended claim 11 because they would not have been obvious. Burns et al. does not teach or suggest using a layer of silicon dioxide that has been implanted with hydrogen ions or the need for a smooth morphology in the polycrystalline layer. The admitted prior art does not mention the formation of a field effect transistor, a memory array or a semiconductor wafer. Thus, amended claim 12 is also nonobvious.

The Examiner asserts that Burns et al. and the applicant's admitted prior art are combinable because they are from the same field of endeavor. The Examiner also expresses that at the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation, as the Examiner claims, is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it is asserted by the Examiner that Burns et al. and applicant's admitted prior art are combinable to obtain the invention of claims 10-12.

Applicant respectfully disagrees that the reference teachings are combinable. The fact that the claimed invention may be within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness. MPEP §2143.01. Some objective reason to combine the teachings of the references must be provided. *Ex parte Levengood*, 28

USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). The Examiner does provide a reason for motivation; however, this motivation is the Examiner's own thought and therefore not objective. Furthermore, the motivation the Examiner provides is not supported by a reference. Thus, the reference teachings cannot properly be combined.

Even if one were to combine the references the present invention would not be taught. As amended, claims 10-12 teach a silicon dioxide layer which is free from metal contaminants. This aspect of the invention is not taught or suggested by either reference. Thus, claims 10-12 as amended are nonobvious.

The Examiner also rejected claim 14 under 35 USC §103(a) as being unpatentable over Murata et al (US Patent No. 5,576,229) in view of applicant's admitted prior art. The Examiner claims that Murata et al. and applicant's admitted prior art are combinable because they are from the same field of endeavor and that at the time of the invention it would have been obvious to a person ordinary skill in the art to implant hydrogen ions into the glass substrate. The Examiner asserts that the motivation for combining the references is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon in order to provide for a thinner and smoother polycrystalline silicon film.

Murata teaches at figure 6E a microcrystalline silicon film 502 that includes source and drain regions 507a and 507b that are doped with impurity ions. Also shown is a channel region 507 not doped with impurity ions that is formed on a substrate 501. An insulating film 503 is formed to cover the microcrystalline silicon film 502. An interlevel insulating film 508 is formed to cover the gate electrode 504. The prior art is explained above.

Claim 14, as amended, recites a thin film transistor that includes a semiconductor substrate that is implanted with hydrogen ions and is free from metal contamination. The cited references do not teach or suggest a semiconductor substrate which is free from metal contamination. Therefore, claim 14 would not have been obvious over Murata in view of applicant's admitted prior art.

Applicant again respectfully disagrees that the reference teachings are combinable. The fact that the claimed invention may be within the capabilities of one of ordinary skill in the art is

not sufficient by itself to establish prima facie obviousness. MPEP §2143.01. Some objective reason to combine the teachings of the references must be provided. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). The Examiner does provide a reason for motivation, however, this motivation is the Examiner own thought and therefore not objective. Furthermore, the motivation the Examiner provides is not supported by a reference. Thus, the reference teachings cannot properly be combined.

Even if one were to combine the references, the present invention would not be taught. As amended, claim 14 recites a silicon dioxide layer which is free from metal contaminants. This aspect of the invention is not taught or suggested by either reference. Thus, claim 14 as amended is nonobvious.

CONCLUSION

Applicant's respectfully submits that, in view of the above amendments and remarks, that amended claims 9-14 are patentable over the cited references and admitted prior art. The application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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